SESSION 18 – TAPA II
Low Power SRAM

Friday, June 18, 3:25 p.m.
Chairpersons: K. Roy, Purdue University
N. Lu, Etron

18.1 — 3:25 p.m.
64Mb Mobile Stacked Single-Crystal Si SRAM (S^3RAM) with Selective Dual Pumping Scheme (SDPS) and Multi Cell Burn-in Scheme (MCBS) for High Density and Low Power SRAM, H.-J. An, H.-Y. Nam, H.-S. Mo, J.-P. Son, B.-T. Lim, S.-B. Kang, G.-H. Han, J.-M. Park, K.-H. Kim, S.-Y. Kim, C.-K. Kwak and H.-G. Byun, Samsung Electronics Co., Ltd., Gyeonggi-Do, Korea

A 64Mb Mobile S3RAM was designed with stacked single-crystal thin film transistor (SSTFT) cell using 80nm SRAM technology to overcome chip size penalty of conventional 6T-SRAM with improved performance. For 1.3V operation, word line (WL) and cell Vcc were pumped simultaneously using selective dual pumping scheme (SDPS). Access time of 49.2ns was achieved at 1.3V supply voltage. Multi cell burn-in scheme (MCBS) and standby current (ISB1) repair scheme enhanced the yield for the high density products

18.2 — 3:50 p.m.
A 0.9ns Random Cycle 36Mb Network SRAM with 33mW Standby Power, H. Pilo, G. Braceras, S. Hall, S. Lamphier, M. Miller, A. Roberts and R. Wistort, IBM Microelectronics, Essex Junction, VT

A 36Mb SRAM with a random cycle of 0.9ns is capable of driving and receiving data at a rate of 1.1Gb/s/pin on input and output pins simultaneously. A sextant architecture provides a 10% improvement in performance over its predecessor. The improved architecture partitions the 36Mb array into non-binary 6Mb sextants. Each sextant supports 1/6th of the 36-bit I/O width. The cycle-time is further improved with a self-timed read to write protocol. High VT array devices reduce array sub-threshold leakage by 22x.

18.3 — 4:15 p.m.
Low Power SRAM Menu for SOC Application Using Yin-Yang-Feedback Memory Cell Technology, M. Yamaoka, K. Osada, R. Tsuchiya, M. Horiuchi, S. Kimura and T. Kawahara, Hitachi, Ltd., Tokyo, Japan

We developed a new "Yin-Yang" feedback technology for SRAM cells, which are composed of six and four transistors with the new D2G-SOI structure. At the 65-nm process node, these cells can operate at 0.7 V in worst case. The operating speeds keep 300 MHz. Leakage current of the four-transistor cell is 1/1000 that of a conventional four-transistor cell. These cells provide an optimal SRAM menu that satisfies the various performance requirements in low-power LSIs.

18.4 — 4:40 p.m.
A Transregional CMOS SRAM with Single, Logic V_{DD} and Dynamic Power Rails, A.J. Bhavnagarwala, S.V. Kosonocky, S.P. Kowalczyk, R.V. Joshi, Y.H. Chan*, U. Srinivasan* and J.K. Wadhwa**, IBM T.J. Watson Research Center, Yorktown Heights, NY, *IBM Systems Group, Poughkeepsie, NY, **IBM Microelectronics Division, Fishkill, NY

Circuit techniques are reported that enable SRAMs to operate at logic VDD witha Read Current and cell Static Noise Margin typically seen in higher/dual VDDSRAMs. Implemented in a 65nm CMOS SOI process, the voltage across accessed SRAM cells self-biases to move them between near-subthreshold and superthreshold regions, lowering total leakage by 10X and improving IREAD and SNM by 7% and 18% respectively with a total area overhead of less than 13%.

18.5 — 5:05 p.m.
A SRAM Design on 65nm CMOS Technology with Integrated Leakage Reduction Scheme, K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng and M. Bohr, Intel Corporation, Hillsboro, OR

4Mb SRAM is designed and fabricated on a high-performance 65nm CMOS technology. It features a 0.57 um2 6T cell with large noise margin down to 0.7V for low-voltage operation. The fully synchronized subarray contains an integrated leakage reduction scheme with sleep transistor. It also has a built-in programmable defect "screen" circuit for high volume manufacturing.